and Claim 8 was rejected under 35 U.S.C. § 103(a) as unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Noda et al.

The abstract of the disclosure has been amended to correct minor informalities. No new matter has been added.

Regarding the rejection of Claim 3 under 35 U.S.C. § 112, second paragraph, Claim 3 has been amended in light of the comments noted in the outstanding Office Action and as shown in the marked-up copy. Accordingly, it is respectfully requested this rejection be withdrawn.

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as anticipated by Noda et al. This rejection is respectfully traversed.

Claim 1 is directed to a semiconductor device including a bonding material disposed on a metal block, between a second surface of a lead frame and the metal block.

In a non-limiting example, Figure 1 shows the bonding material 10 disposed on the the metal block 5 between the second surface of the lead frame 2a and the metal block 5.

The present invention advantageously provides a metal block in a semiconductor device so to dissipate a heat generated from a power element at a high rate.[1]

Noda et al disclose a semiconductor device as shown in Figures 1 and 2 having a circuit pattern layer 106 provided on a second surface of a lead frame 103a. Noda et al state at column 8, lines 60-61 "The circuit pattern layer 106 is formed of, for example, copper and aluminum cladding foils." In other words, the circuit pattern layer 106 in Noda et al is very thin in contrast to the metal block recited in Claim 1. The fact that the metal block 5 is not a foil is consistently described in the specification at page 4, lines 7-10, page 12, lines 15-18 and page 12, lines 22-24. As the metal block of the present invention has a sufficient

[1]See specification, page 11, line 9 to page 12, line 9.

thickness and a high heat diffusion due to its thickness, Applicant respectfully submits the foil circuit pattern 106 in Noda et al cannot achieve the advantages of the present invention.

Furthermore, since the lead frame 2A of the present invention is not a foil but rather a sheet, as described at page 10, line 6, the heat diffusion properties of the lead frame are superior comparative to the circuit pattern 106 in Noda et al which is formed on a foil. Thus, Noda et al do not teach or suggest a block metal, but a foil.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

In addition, regarding the rejection of Claim 7 over Noda et al, Applicant notes Noda et al disclose a first surface of the circuit pattern layer 106 is closer to a lead frame 103 then a second surface of the circuit pattern layer 106. Figure 1 of Noda et al shows the first surface of the circuit pattern layer 106 corresponds to the upper surface of the circuit pattern layer 106 and the second surface of the circuit pattern layer 106 corresponds to the lower surface of the circuit pattern layer 106, i.e., a bonding surface to insulation layer 105. In other words, the first and second surfaces of the circuit pattern layer 106 are opposite to each other.

However, the present invention teaches that both the first and second surfaces of the metal block are opposite from the insulation layer 60 and therefore on a same surface of the metal block 5. Therefore, Noda et al do not teach or suggest first and second surfaces of a metal block on a same side of the metal block.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as unpatentable over AAPA in view of Noda et al. This rejection is respectfully traversed.

Claim 8 depends directly on independent Claim 1, which as discussed above, is believed to be allowable. Therefore, it is respectfully submitted Claim 8 is also allowable.

In addition, Claim 8 recites three surfaces of the lead frame 2A, for example in Figure 7, so that the third surface corresponding to the non-bonding surface 53 is closer to the semiconductor element as viewed in a vertical direction to the semiconductor element then the second surface corresponding to the bonding surface 52. Further, the second and third surfaces of the lead frame of the present invention are on the same side of the lead frame 2A, as shown in Figure 7.

Thus, AAPA does not teach or disclose three surfaces of the lead frame so that two of the surfaces are on the same side of the lead frame and the third surface closer to the semiconductor element, as viewed in the vertical direction to the semiconductor element, than the second surface.

Noda et al do not suggest to modify the surfaces of the lead frame for having three surfaces disposed as indicated above. Therefore, it is respectfully submitted the combination of AAPA in view of Noda et al does not render obvious the invention defined by amended Claim 8.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Gregory J. Maier
Attorney of Record
Registration No. 25,599
David A. Bilodeau
Registration No. 42,325

22850

(703) 413-3000
Fax #: (703)413-2220
GJM:DAB:RFF\ses
I:\atty\Rff\210314\210314us-am2.wpd

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IN THE CLAIMS

Please cancel Claims 9-11 without prejudice.

Please amend Claims 1, 3 and 5-8 as follows:

--1. (Amended) A semiconductor device comprising:

a semiconductor element;

a lead frame having a first surface [for mounting] on which said semiconductor element is mounted [thereon], and a second surface opposite [from] to said first surface;

a metal block [provided] on said second surface of said lead frame;

an insulation layer [provided] on said metal block opposite said lead frame; and

a bonding material between said second surface of said lead frame and said metal block,

wherein said bonding material [being better in] has a higher heat conduction than said insulation layer.

3. (Amended) The semiconductor device according to claim 1,

wherein said metal block has a wider surface opposite said bonding material than said bonding material [opposite said bonding material].

5. (Amended) The semiconductor device according to claim 1, further comprising:

a resin package [for sealing] configured to seal said semiconductor element, said lead frame and said metal block while uncovering said insulation layer,

wherein said insulation layer [is better in] has a higher heat conduction than said resin package.

6. (Amended) The semiconductor device according to claim 5,

wherein said insulation layer comprises a base material with [the] a same base as said resin package, and ceramic powder.

7. (Amended) The semiconductor device according to claim 1,

wherein said metal block has a first surface and a second surface opposite said insulation layer,

wherein said first surface of said metal block is closer, as viewed in [the] a vertical direction, to said lead frame than is said second surface of said metal block, and

wherein said bonding material lies between said second surface of said lead frame and said first surface of said metal block.

8. (Amended) The semiconductor device according to claim 1,

wherein said lead frame has a third surface on the same side as said second surface, [and]

wherein said third surface is closer, as viewed in [the] a vertical direction, to said semiconductor element than is said second surface [to define], and

wherein an insulation space is defined between said metal block and said third surface.--

IN THE ABSTRACT

Page 24, lines 3-14, please amend the abstract to read as follows:

A lead frame [(2a)] has a die bonding pad portion [(3)] and an inner lead portion [(4)]. A power element [(1)] is mounted on the die bonding pad portion [(3)] of the lead frame

[(2a)] and is bonded to the die bonding pad portion [(3)] with a solder [(9)]. The power element [(1)] has electrodes connected through an aluminum wire [(8)] to the inner lead portion [(4)] of another lead frame [(2b)]. A metal block [(5)] has a surface formed with a protrusion bonded to the lead frame [(2a)] in opposed relation to the power element [(1)]. A resin package [(6)] has an insulation layer [(7)] formed on [the] an opposite surface of the metal block [(5)] from the lead frame [(2a)], and seals the power element [(1)], the lead frames [(2a, 2b)] and the metal block [(5)]. An external heat dissipator [(11)] is mounted on a surface of the insulation layer [(7)] opposite from the metal block [(5)]. A semiconductor device and a method of manufacturing the same improve a heat dissipation characteristic and maintain a dielectric breakdown voltage.--